REMARKS

Applicants respectfully request reconsideration of the above identified application. Claims 1-46 are pending. Claims 1-46 are rejected.

The remaining comments are directed to Claim 1-46. The Office Action mailed on April 3, 2003 rejects Claims 1-15 and 19-46 under 35 U.S.C. 102(e) as allegedly being anticipated by Yoshioka et al., U.S. Patent 6,138,226.

The Examiner states with respect to Claims 1-3, 5-10, 12 and 31-34 that, "Yoshioka discloses a method, executable code and processor for transparently sharing virtual address translations, by accessing a translation and identifying if it is sharable...the shared flag SH identifies if the translation is sharable, and this procedure is transparent to the OS to the extent claimed, since as seen in Figure 1, in both the logical cache 10 and in the TLB, a shared flag indicates if the translation may be shared without communicating this to the OS...;" with respect to Claims 13, 15, 19-22 and 28-30 that, "Yoshioka discloses processors and logical processors as recited;" and with respect to Claims 24-27, 35-36, 40 and 42-46 that, "Yoshioka discloses the TLB stores the indication."

Applicants respectfully disagree with the Examiners assertions. Claims 1, 9, 13, 20 and 35 set forth sharing virtual address translations. Similarly Claims 31 and 36 set forth sharing entries to translate virtual addresses to physical addresses.

Yoshioka, on the other hand, does not share the virtual address translations or the entries to translate virtual addresses to physical addresses. Instead, Yoshioka discloses that multiple virtual address translations, which

produce the same physical address, are stored and are used to determine when one logical address shares data with another logical address, by comparing the physical addresses produced by the respective virtual address translations.

For example, Yoshioka discloses with respect to Figs. 1 and 2, in col. 7 lines 1-20 [emphasis added]) that:

> Namely, the <u>logical address b</u> as a search address of the cache memory 10 <u>is subjected to address translation by means of the TLB 11</u> to obtain its physical address information PA (b). The <u>physical page information PA(b) is compared with the physical page information PA(a)</u> retained by the entry thus selected. <u>In a case where the cache entry has no physical page information as shown in FIG. 2, TLB has to be accessed to translate logical page information in the entry thus selected into physical page information. Therefore, the number of times access is provided to the TLB 11 is halved in this embodiment of the invention in comparison with that of FIG. 2</u> and power consumption becomes reducible to that extent.
>
> <u>When a comparison between both the physical addresses results in a good match, that is, PA(a)=PA(b),</u> data in the entry is used as a cache hit because <u>it is assumed that the logical address b shares data with the logical address a.</u> Consequently, a <u>plurality of data assigned to the same physical address</u> are prevented from existing in the logical cache memory and the problem of a synonym is solved.

Applicants respectfully submit that Yoshioka does not disclose or suggest methods of sharing virtual address translations or entries to translate virtual addresses to physical addresses, but rather discusses resolving the synonym problem wherein multiple virtual address translations are assigned to the same physical address. Further, Yoshioka does not disclose or suggest that there may be cases in which virtual address translations or entries to translate virtual addresses to physical addresses could be shared.

Therefore, Applicants respectfully submit that Claims 1, 9, 13, 20, 31, 35 and 36 are patently distinguished over the art cited by the Examiner. Applicants further believe that Claims 2-8, 10-12, 14-19, 21-30, 32-34 and 37-46 being

dependent therefrom are also patentable. Applicants respectfully request the Examiner withdraw his rejection under 35 U.S.C. 102(e).

The Office Action further rejects Claims 16-18 under 35 U.S.C. 103(a) as allegedly being unpatentable over Yoshioka.

Applicants respectfully disagree with the Examiners assertions with regard to the obviousness of shared caches. However, in light of the arguments presented above, Applicants respectfully submit that the larger issue is that Yoshioka does not even disclose or suggest that a virtual address translation may be shared. Therefore Applicants respectfully request the Examiner also withdraw his rejections under 35 U.S.C. 103(a).

Applicants, therefore, believe that Claims 1-46 are presently in condition for allowance and such action is earnestly solicited.

CONCLUSION

Applicants respectfully submit the present claims for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Lawrence M. Mennemeier at (408) 765-2194.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

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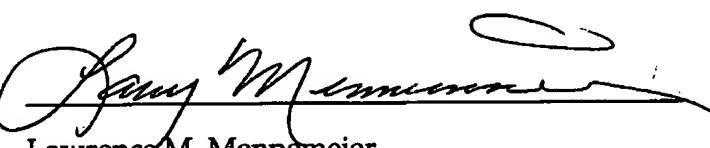
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